



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: Unassigned
Examiner: Unassigned

In Re PATENT APPLICATION Of:

Applicant : Hirotaka KOMATSUBARA)
Serial No. : 10/765,156)
Filed : January 28, 2004)
For : SEMICONDUCTOR DEVICE AND METHOD)
FOR MANUFACTURING THE SAME)
Attorney Ref. : KAN 155)

**INFORMATION
DISCLOSURE
STATEMENT**

April 9, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an Information Disclosure Statement submitted in compliance with the timing requirements of 37 C.F.R. § 1.97(b)(1), i.e. within three months of the filing date of the application.

Attached are copies of two English-language articles, which are discussed on pages 2 and 3 of the present application, and which are listed on the attached Form PTO-1449. Any relevance of the articles is self-evident.

Since this Information Disclosure Statement is being filed within three months of the filing date of the application, no certification or fee is required, and the requirements of 37 C.F.R. §§ 1.97 and 1.98 are deemed to be fully met as to all listed documents. Consideration of the listed documents is respectfully requested.

Respectfully submitted,

Robert H. Berdo, Jr. (Reg. No. 38, 075)
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April 9, 2004
Date

RHB:vm

FEE ENCLOSED: \$
Please charge any further
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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT				Atty. Docket KAN 155		Application No. 10/765,156	
				Applicant Hirotaka KOMATSUBARA			
				Filing Date January 28, 2004		Group Unassigned	
U.S. PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Name	Class	Sub-Class	Filing Date
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Sub-Class	Translation
	AI						
	AJ						
	AK						
	AL						
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AM	OKANO et al., Fabrication of a Miniature-Size Pyramidal-Shape Diamond Field Emitter Array, IEEE ELECTRON DEVICE LETTERS, VOL. 16, NO. 6, JUNE 1995					
	AN	KANG et al., Reduction of Leakage Current at the Gate Edge of SDB SOI NMOS Transistor, IEEE ELECTRON DEVICE LETTERS, VOL. 16, NO. 6, JUNE 1995					
Examiner					Date Considered		
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							